



Compiling A Project In Quartus II



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YouTube

<https://youtu.be/uPuui9ZhZk8>

Website

<http://fpga.seanwrall.com/lessons/lesson3/>

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Documentation Written By Sean W. Rall



Revision History

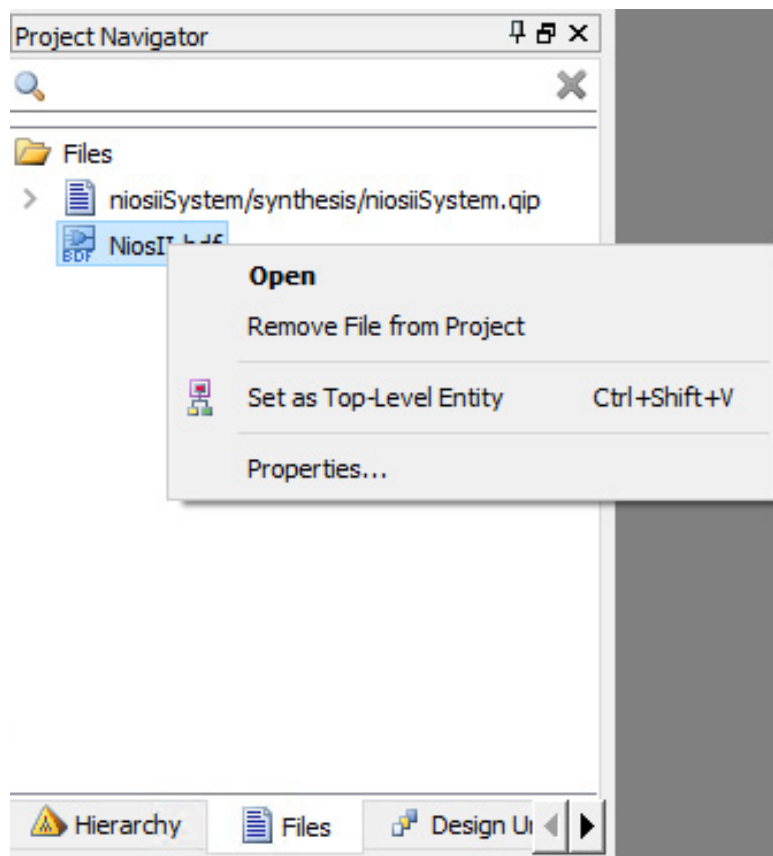
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No Updates



Quartus II Setup

1. Navigate to your project directory (in this case C:/altera/mySystems/system1)
2. Open the Quartus project file (.qpf) in our case NiosII.qpf
 - A. Quartus Should now open with your project
3. Double click on NiosII under the "Entity" window on the left
 - B. This should have a opened the NiosII.bdf file in the center of Quartus II
 - C. If NiosII is not your top level entity (ie: shows as the highest element in the entity windows) preform the following, if it is the top most entity already then skip to step 4
 - i. In the left hand pane next to Hierarchy click on Files
 - ii. Right click on NiosII.bdf
 - iii. Select Set as Top-Level Entity As shown below





Quartus II Setup

4. Go to Project --> Add/Remove Files in Project...
 - A. In the settings pop up go to Files
 - B. Next to filename click on the ... icon 
 - i. Find NiosII.bdf (note this file might already be added, if it is already added skip to step iv)
 - ii. Click open
 - iii. Click add
 - iv. Find niosiiStsyem.qip (the file we generated in Qsys located in system1/niosiiSystem/synthesis) You might have to change the file type to IP Variation (.qip .sip)
 - v. Click open
 - vi. Click add
 - C. Click Apply
 - D. Click OK
5. Go to Assignments --> device
 - E. Click device and pin options
 - F. Click Unused Pins
 - i. For Reserve all unused pins select As input tri-stated



Adding A Block Diagram

1. Double Click on the work space area (the area with a dot pattern)
 - A. In the Symbol popup menu under name click the ... button 
 - B. Navigate to the niosiiSystem.bsf that we created in Qsys (system1\niosiiSystem)
 - C. Select niosiiSystem.bsf
 - D. Click open
 - E. A preview should now appear in the symbol popup
 - F. Click OK in the symbol popup
2. Place the block diagram anywhere on the workspace by clicking



Adding Pins By Using A Defined .qsf File

1. Navigate to your project folder and find the file niosll.qsf (system1\niosll.qsf)
2. Open the .qsf file in a text editor like notepad
3. At the bottom of the file past in the contents of the .qsf file found at <http://fpga.seanwrall.com/lessons/lesson3/> (Download DE2-115 .qsf file addon (TXT))
 - A. Save the file
4. Place a pin by clicking on  Add a pin in the workspace tool bar
 - A. Select the pin you need from the drop-down (input, output, bidirectional)
 - B. Place the pin by clicking on the workspace where you want the pin to be placed
 - C. When done placing the pin press Esc to stop placing more pins
 - i. For this example we need two inputs and one output
5. Connect the pins to the device by dragging from the device to the pin (not from the pin to the device)
6. Name the pins the corresponding values in the .csv file found at <http://fpga.seanwrall.com/lessons/lesson3/> (Download DE2-115 Pin Assignment (CSV))
 - A. For us the clk_clk should be named CLOCK_50
 - B. For us the green_leds_export[7..0] should be named LEDG[7..0]
 - C. For us the reset_reset_n should be named KEY[0]

Note: Pin names are case sensitive

Note: to make multiple bit connections to one pin use the format "PINNAME[X..Y]" where X is the most significant bit and Y is the least significant bit

Green Lines are Bidirectional Pins

Blue Lines are Input Pins

Purple Lines are Output Pins



Compiling/Generating A Quartus Project

1. Click start compilation  (the purple arrow in the toolbar)
2. The progress of the compilation will be shown in the lower left and in the console window at the bottom
3. When done the console window will display Quartus II Full Compilation was successful. 0 errors
 - A. You do not want errors here but warnings are OK